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3D integrated system for advanced intelligent computing

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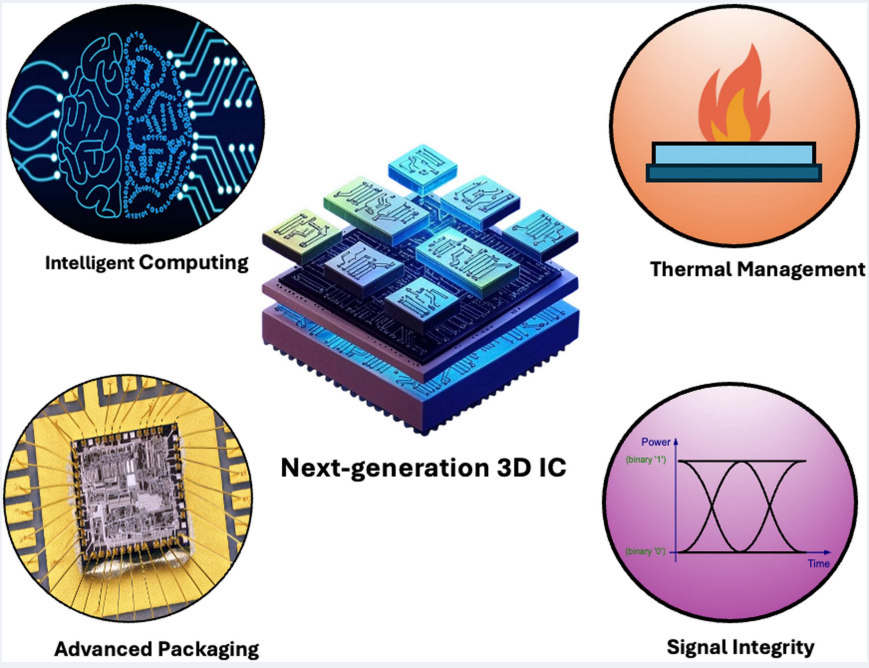
ABSTRACT

Emerging technologies such as artificial intelligence (AI), large-scale molecular simulations, and next-generation materials and drug discovery demand unprecedented computational power and high-bandwidth interconnects. Conventional two-dimensional integrated circuits (2D ICs) are nearing their physical and performance limits due to challenges in thermal management, signal integrity, and leakage currents. Three-dimensional integrated circuits (3D ICs) offer a promising pathway to overcome these limitations by vertically stacking multiple device layers, thereby reducing interconnect lengths and enabling a broad range of high-performance applications. This paper presents a comprehensive review of 3D ICs systems, with an emphasis on energy efficiency across various conventional and heterogeneous integration schemes, packaging architectures, and the trade-offs between thermal and electrical performance. We examine the relative merits of different bonding techniques, floorplanning algorithms, cooling solutions, and power delivery network (PDN) designs, highlighting their interdependencies and optimization challenges. The insights presented in this review are intended to help researchers and designers identify and implement strategies that enhance the performance, energy efficiency, and reliability of 3D ICs for high-performance computing applications.



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1 Introduction

Microprocessor technology has seen great development since its inception in the 1960s. The primary driving force behind this advancement has been the scaling of silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs), which has enabled transistor dimensions to shrink from several millimetres to just a few nanometres. Moore's law has been the guiding beacon for this enormous progress in scaling, which stated that the number of transistors doubles approximately every two years [1]. While Moore's law did not mention anything about the physical scaling of the transistors, the doubling of the number of transistors was guided by Dennard scaling, which stated that as transistors scale, their clock frequency increases while power consumption remains constant [2,3]. Unfortunately, this scaling lasted until 2005-2006, since when clock frequency stopped increasing because of high dynamic energy that scales as the square of clock frequency [4]. Subsequently, architectural scaling emerged through the introduction of multi-core modules within the chip [5]. The impact of this trend on human life has been nothing short of remarkable. However, like every trend, this scaling approach is reaching its limits. Packaging limitations, particularly lithographic constraints, have become more pronounced in recent years, making it extremely difficult to pack more transistors at the nanoscale. Even advanced lithographic techniques have become prohibitively expensive for most fabrication facilities, leaving only a few competitive fabs remaining in the market [6–8]. Furthermore, the scaling of physical dimensions of the device comes at a cost of interconnect delay, reduced signal integrity, and heat dissipation issues to the extent that these bottlenecks hinder the growth of two-dimensional integrated circuits (2D ICs). With the advent of artificial intelligence (AI) models experiencing a 10× increase in the number of parameters per year, and the growing requirements for high performance with low power consumption, today's multi-core 2D IC architecture has been driven to its physical and economic limits. Therefore, the use of the third dimension for scaling is inevitable [9–12].

Three-dimensional integrated circuits (3D ICs) offer efficient scaling by harnessing the vertical dimension for stacking multiple active die layers interconnected through high-density vias or Cu-Cu die bonding. This approach significantly improves computing performance by reducing total interconnect length, signal delay, and footprint. 3D ICs provide improved memory bandwidth by allowing the stacking of multiple primary or cache memory units, resulting in the increase of the available memory capacity [13,14]. Early research results have demonstrated the transformative potential of 3D ICs in alleviating interconnect bottlenecks and supporting the development of advanced system-on-chip (SoC) architectures [15–17]. Recognising this trend, there has been increased interest in adopting 3D design in dynamic random-access memory (DRAM), in the form of high bandwidth memory (HBM), which has been industrially adopted by companies like Micron and SK Hynix since 2015 [18] to handle the AI training load in datacenters. State-of-the-art advancements in 3D IC technology, such as AMD's 3D V-Cache, TSMC's SoIC and Intel's Foveros architectures (see Figure 1a), demonstrate the commercial viability of advanced stacking technology [19–22]. With 3D integration, Moore's original law is not obsolete; rather, it has gained an additional dimension as depicted in Figure 1b. However, this added dimension brings both opportunities and challenges. This paper discusses these challenges and examines important emerging trends in 3D ICs technology.

2 Intelligent computing driven by 3D integrated systems

The acceleration of the discovery and creation of knowledge in recent history can be largely attributed to the accessory intelligence obtained through the advancement of artificial intelligence (AI) enabled by microelectronics. Initially, massively improved communication and computational aid enabled by a predominantly man-focused relationship with machines stimulated this growth. The power of this collaboration drove rapid innovation of machines, both in software and hardware forms. This innovation has pushed the boundaries of intelligent systems to incredible horizons. For instance, In 2016, the inflection point came when AlphaGo, an AIcomputer programme by DeepMind, defeated Lee Sedol, the top human Go master [23].

The growth of intelligent computing began with feature scaling, underwent the era of 2D, multicore expansion, and has begun vertical aggregation in response to the physical and economic limitations. Planar architecture is hindered by the inherent complications of making off-chip interconnectivity [24]. As AI is applied to emerging landscapes with evolving requirements for processing speed, data storage, and energy

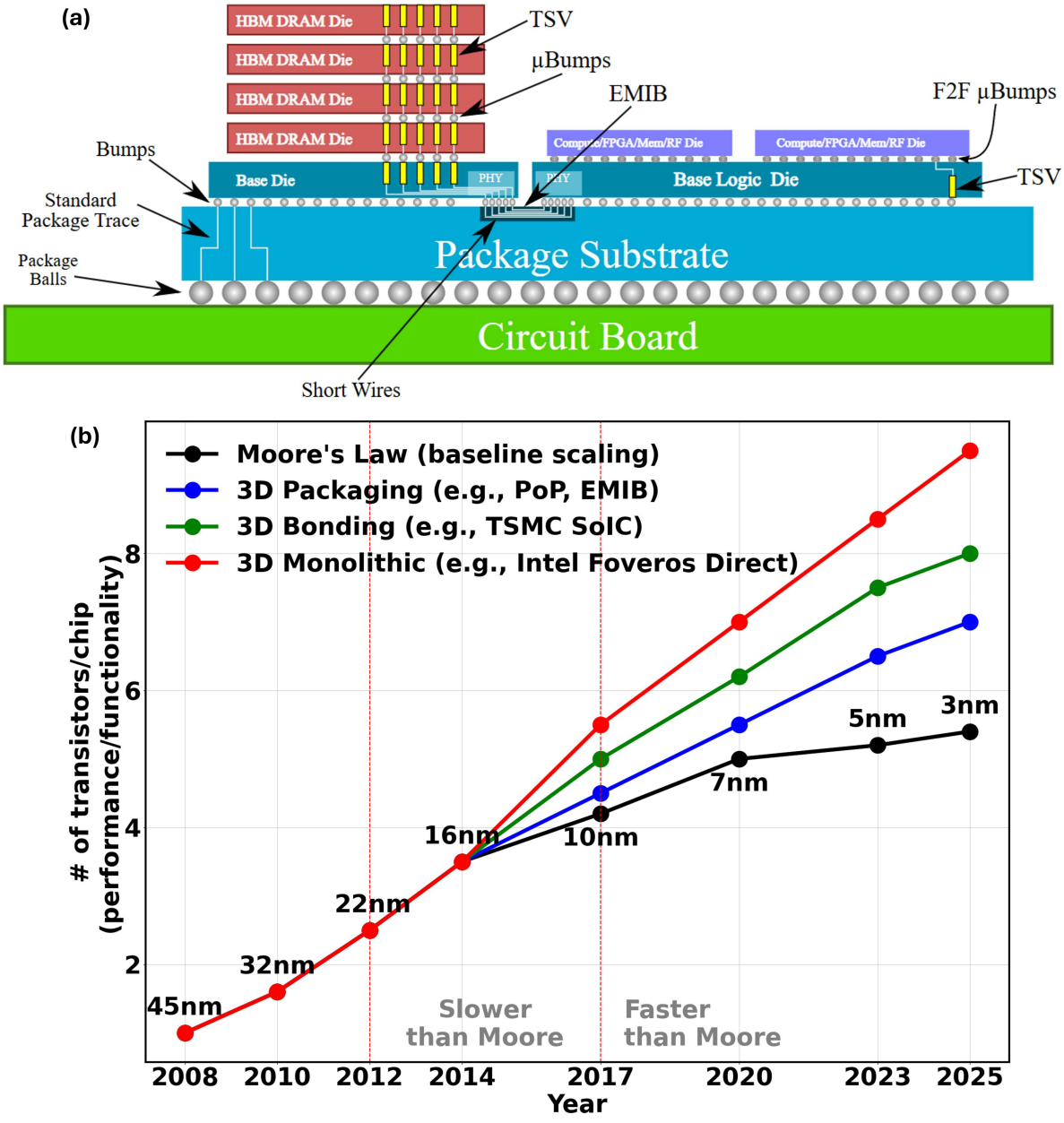

Figure 1. (a) Foveros is a high-performance 3D IC face-to-face (F2F) based packaging technology designed by Intel [19] (b) 3D ICs Performance with diffrent node technologies (reproduced with permission from [20]).

efficiency, inefficiencies resulting from the need of increasing off-chip communication (termed as Von Neumann bottleneck) is going to be unsustainable in the near future [25]. Instead, system-level optimisation of the full computing stack drives 3D integration by increasing interconnect density, minimising power dissipation, and improving memory bandwidth, thus providing high-capacity, low-cost opportunities for the future (Figure 2) [24,26].

For training an intelligent computational model requires significant investment in both energy and money, owing to the introduction of Kaplan scaling, which asserts that performance improvements are a result of an increase in the number of parameters an AI solution utilises [27]. Scaling the number of parameters is enabled by chips having fast access to memory which stores the massive datasets required for training. 3D integration poses a solution to the bottlenecks of off-chip memory by improving the memory bandwidth with vertical stacking and increasing interconnect density. To further the abilities of intelligent computing, 3D integration also provides benefits through the heterogeneous integration (HI) of

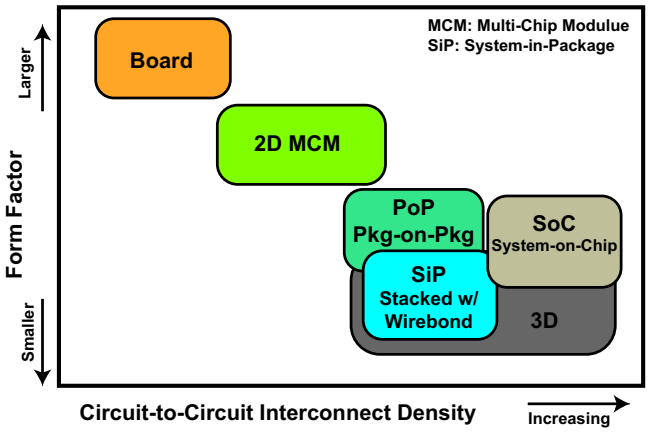

Figure 2. Form factor and interconnect density improvements of various packaging technologies (reproduced with permission from [24]).

technologies. HI means packaging chips of different functionalities, feature sizes, and even fabricated in different fabs into a single unified system to improve performance. This modularity of design speeds up commercialisation, reduces cost, and eases IP challenges [28]. The ability to combine technologies on single chips through 3D integration provides better coordination of storage, communication, and computation to accelerate the development of intelligent computing and large scale AI models (Figure 3) [23,29].

3 Packaging of 3D ICs

Packaging and assembly are key building blocks of any commercial technology. Several approaches are adopted for the packaging of 3D ICs, including monolithic 3D integration, direct oxide wafer bonding, metal bonding using through-silicon-vias (TSVs) and recently developed self-assembly based integration [20]. Table 1 provides a comparative analysis of 2D, 2.5D, and 3D packaging solutions. In the process of monolithic integration, devices are connected by interlayer vias and stacked on the same wafer. The vias in monolithic 3D integration are fine, which avoids the application of a keep-out zone and reduces the concern of induced mechanical stress [30]. However, the device stacking sequence in monolithic 3D integration is limited to thermal budgets. To prevent damaging the bottom layers, the devices on the top layers must have a lower thermal budget. In recent studies of monolithic 3D integration, two-dimensional semiconductors [31,32] and oxide semiconductors such as indium-gallium-zinc-oxide (IGZO) and indium-tin-zinc-oxide (ITZO) [33,34] have shown potential due to their lower processing temperatures and compatibility with back-end-of-line (BEOL) processes.

The most promising packaging solution for 3D ICs is the use of TSVs for bonding of die from different layers. Compared with monolithic 3D integration, the stacking sequence in TSVs is not strictly limited by thermal budgets because the chips are connected by through-silicon vias after fabricating devices on individual chips. In TSV formation processes, chemical mechanical planarization (CMP) is commonly applied to improve stress uniformity, eliminate Cu protrusion, and avoid package warpage [35,36]. Various materials can be used for bonding formation, including metal, oxide, and polymer. Metal bonding enables chips to be electrically connected, which is conventionally formed by thermal compression. Cu is the widely used metal due to its outstanding thermal and electrical properties. However, direct Cu-Cu bonding formation requires high temperature, which may not meet the thermal budget. Efforts have been made to lower the bonding temperature, such as applying hybrid bonding, surface-activation bonding, passivation layers, and other novel bonding methods. Figure 4 shows the trend of approaching lower processing temperatures in TSVs. Direct oxide bonding mainly serves as insulating layers, which can be formed at room temperature via van der Waals forces. Nevertheless, this kind of bonding typically requires further annealing to high temperatures to increase stability. Polymer bonding mainly serves as adhesion layers, which play an important role in providing mechanical support. Due to the larger size of vias, wafer thinning and keep-out zones are required in TSVs packaging. Wafer thinning not only assists with the

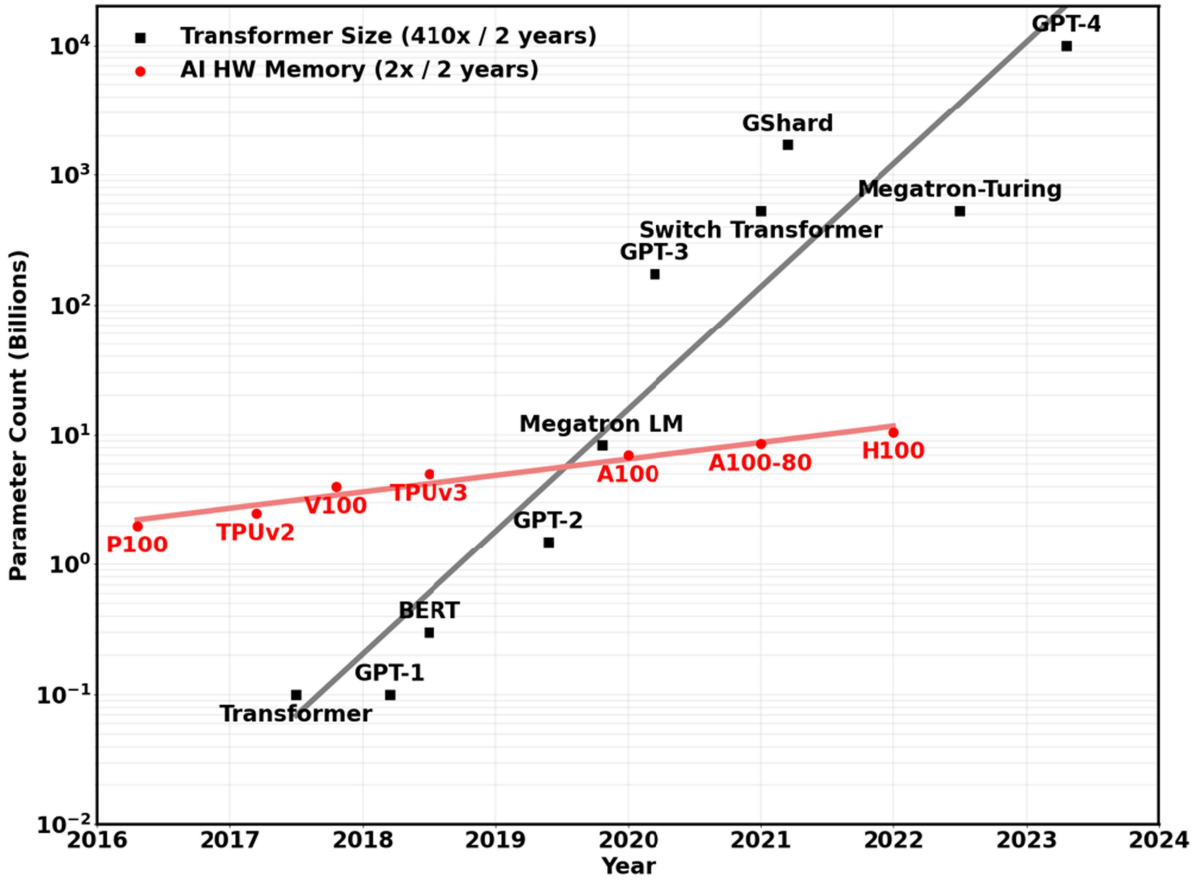

Figure 3. Evolution of the number of parameters used in state-of-the-art models (black) and memory capacity (red). The number of parameters utilised in transformer models increases by 410× every 2 years while the memory capacity only grows at 2× every 2 years. GPU memory is plotted by dividing memory size by six as approximate upper bound of the largest model which can be trained with corresponding memory (adapted with permission from [29]).

Table 1. Comparison of 2D, 2.5D and 3D packaging techniques.

Packaging type	Advantages	Disadvantages
2D (planar packaging)	Mature packaging, low cost, high yield, simple processing	Long interconnections, low interconnect density, high power consumption
2.5D (interposer-based)	High bandwidth interconnections, easier thermal management compare to 3D solutions	Limited vertical integration, interposer increases the cost
3D TSV-based	BEOL compatible, heterogeneous integration allowed	Vias are large, keep-out zones are required, difficult uniform Cu via filling, Thermal challenges
3D Monolithic	Ultra-thin and dense vertical interconnections, heterogeneous integration allowed	Difficult thermal budget management, high process complexity
3D Hybrid bonding	Fine-pitch, high-density interconnections	High alignment difficulty, CTE mismatch

*BEOL: Back end of line, CTE: Coefficient of thermal expansion.

miniaturisation of IC packaging but also enables the vias to connect both sides of the wafer. However, wafers tend to become fragile after the wafer thinning process. Therefore, chips are often temporarily bonded and de-bonded on a carrier wafer through heating or exposing polymer adhesive layers to ultraviolet lasers [37,38]. For instance, photosensitive polyimide [39], Brewer Science polymer [40] are reported in recent studies.

4 Design methodologies for thermally efficient 3D ICs

3D ICs technology offers many advantages compared to 2D ICs designs. However, the vertical integration of multiple active layers results in increased power densities, consequently leading to higher on-chip

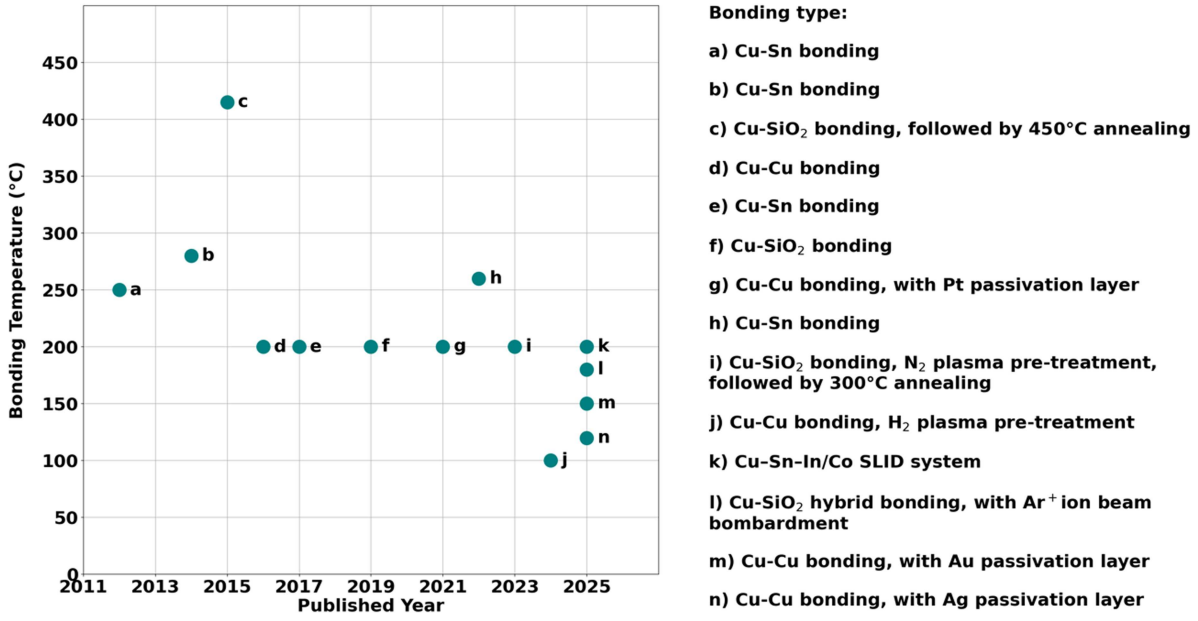

Figure 4. Approaches to lowering bonding temperatures in TSV packaging. This data is obtained from [41–54].

temperature [55,56]. High on-chip temperature can have adverse effects on the performance and reliability of the stacked system. Reliability issues such as electromigration (EM) and negative-bias-temperature instability (NBTI) become more pronounced with increasing temperature [57–59]. As discussed in section 3, formation of defect-free TSVs is critical to achieving better performance, and this can be achieved by reducing wafer thickness. However, reduction in wafer thickness can limit heat dissipation through the wafers due to phonon scattering at the interface layers [60]. Phonon scattering becomes dominant at higher temperatures, resulting in increased interconnect delay and leakage power, and can even lead to thermal runaway. The stacked system also consists of dielectric and adhesive bonding materials, which essentially limit the heat transfer paths due to their high thermal resistances [61]. In 3D ICs, the bottom side is generally equipped with electrical circuits, so only the top side may be available for heat dissipation for state-of-the-art cooling techniques. Therefore, implementing thermal-conscious design methodologies is crucial for efficient 3D ICs development. Here, we review recent studies on thermal designs for 3D ICs and discuss their solution schemes to overcome thermal challenges through efficient engineering.

Conventionally, hotspot measurements of active chips can be conducted using experimental techniques such as Infra-red Thermography (IR), Thermoreflectance (TR) Microscopy, Scanning Thermal Microscopy (SThM) etc [62]. However, in 3D ICs, it is very challenging to conduct heat measurements for each individual die or layer [63]. Therefore, for accurate prediction of the temperature of each layer, the development of a corresponding heat transfer model is essential. There are various analytical and numerical approaches that are reported in the literature for modelling 3D ICs heat transport processes [64,65]. In 3D ICs, floorplanning, TSV placement, and routing are key important steps, and these steps should account for thermal-electrical co-design and co-optimisation [66]. Athikulwongse et al. developed a TSV spread and alignment algorithm to form a uniform thermal conductivity space and increase vertical overlap among TSVs across the dies in a 3D stack [67]. TSVs help dissipate power efficiently, so it is advantageous to position TSVs close to cells that dissipate high power density. Therefore, spreading TSVs according to cells' power-density dissipation may reduce local temperature and intra-die thermal variation in 3D ICs. Furthermore, this algorithm helps align TSVs from die to die to avoid heat constriction paths from TSV-adhesive or TSV-die interfaces (see Figure 5). Thermal-aware floorplanning is an inevitable step in the 3D IC design flow, as it involves determining the position of each cell on the wafer. Numerous design algorithms based on finite difference method (FDM), finite element method (FEM), B*-tree, relaxed conflict net (RCN), and deep reinforcement learning have been proposed to enable thermal-aware floorplanning of 3D ICs [64,68,69]. In general, the weighted total interconnection wirelength (L_w) is

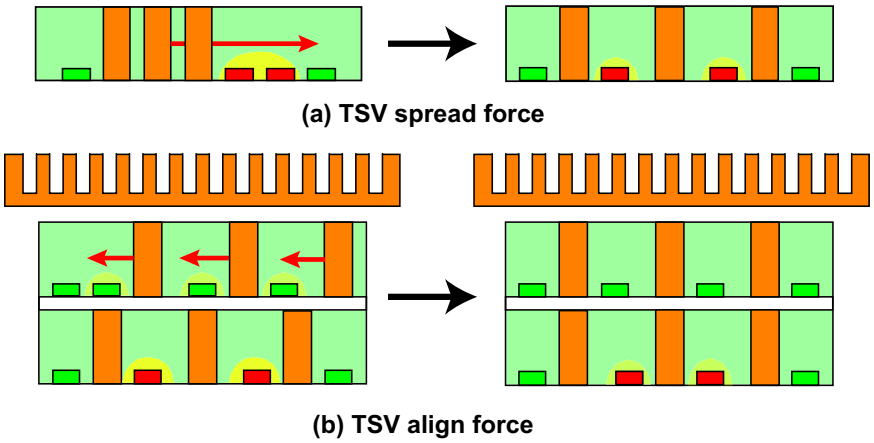

Figure 5. (a) TSV Spread and (b) TSV Align algorithm based on power-density force optimisation (reproduced with permission from [67]).

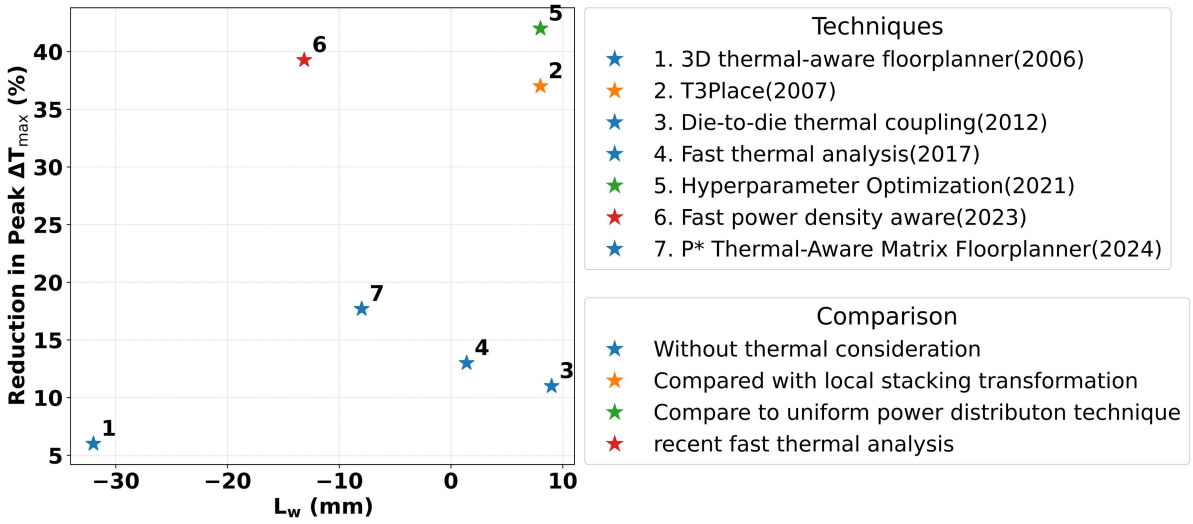

Figure 6. Reduction in peak temperature (ΔT_{max}) of top tier die and interconnection length (L_w) reduction showed by different algorithms. This data is taken from [67–74].

widely accepted as the metric to evaluate the quality of different techniques. Therefore, in thermally aware placement, temperature is managed as a penalty to the wire-length (L_w) objective function [64]. Figure 6 shows hotspot reduction (ΔT_{max}) and corresponding interconnection length (L_w) reduction demonstrated by several floorplanning optimisation techniques from the recent reports in literature.

In 3D ICs, it is challenging to remove heat from intermediate layers with increasing numbers of stacked layers. A major concern is that the Si-layer with thickness <1μm exhibits a 2-fold lower thermal conductivity than its bulk form [75]. Therefore, 3D ICs cannot rely on spontaneous heat dissipation through Si. If the heat is not removed efficiently, thermomechanical stress arises around the TSVs due to the generated thermal gradients, which leads to serious reliability concerns [76]. Conventional cooling techniques such as air-cooling, liquid-cooling, backside heat exchangers, or thermoelectric coolers are not appropriate choices for 3D ICs because of their inability to reach intermediate layers. Therefore, it is crucial to develop efficient thermal management strategies and cooling techniques to unlock the full potential of stacked systems. The material choice of dielectrics and adhesives is the rate-determining step of heat transfer through layers. Köroğlu et al. proposed replacing the thermally resistive interlayer dielectrics with high thermal conductivity electric

insulators such as AlN and hexagonal BN (hBN). AlN is an isotropic, high thermal conductivity material that efficiently removes heat from intermediate layers of a 3D stack. Whereas hBN is a strongly anisotropic, high thermal conductivity material that helps reduce hotspot peak temperatures [77].

All 3D ICs design options face the challenge of ineffectiveness in removing heat from the intermediate heat-dissipating layers. Most techniques rely on an array of TSVs [61]. Wei et al. developed a power delivery networks (PDNs) based framework for delivering noise-free power which also contributes to the heat removal from intermediate layers [78]. This PDNs framework uses the inter-layer vias (ILVs) for connecting different components belonging to different layers of 3D ICs. Their simulation results show that PDNs can reduce the maximum steady-state temperature by 35 °C for a 2-layer monolithic 3D IC. In the last few years, a significant number of researches have demonstrated the high performance of microchannel liquid cooling technique through a variety of architectures [79–81]. For example, Tiwei et al. proposed a novel impingement-based liquid cooling solution, fabricated using low-cost polymer, to directly cool the backside of high-performance chip stacks in 3D ICs [82]. Furthermore, Wu et al. from TSMC invented a direct silicon-water cooling solution for ultra-high-power cooling for 3D ICs as shown in Figure 7. This technique successfully demonstrated high cooling performance with total power >2600 W on a single silicon-on-Chip (SoC), equivalent to the power density of 4.8 W/mm^2 [83]. Modelling of thermal optimisation of 3D ICs requires heavy computational power due to the requirement of solving large partial differential equation (PDEs) systems. Recently, a variety of PDE solution schemes have been developed to solve complex geometries of 3D ICs architectures with appropriate boundary conditions. Liu et al. proposed a neural network-based framework named DeepOHeat. This is a physics-aware deep learning model to predict temperature fields in 3D ICs [84]. Table 2 shows a few recently developed cooling approaches and their corresponding outcomes. With these strategies, it is important to experimentally validate each technique and find a cost-effective thermal management solution for 3D ICs. The decision of which thermal management technique to implement for a specific chip design is dependent on its application and cost.

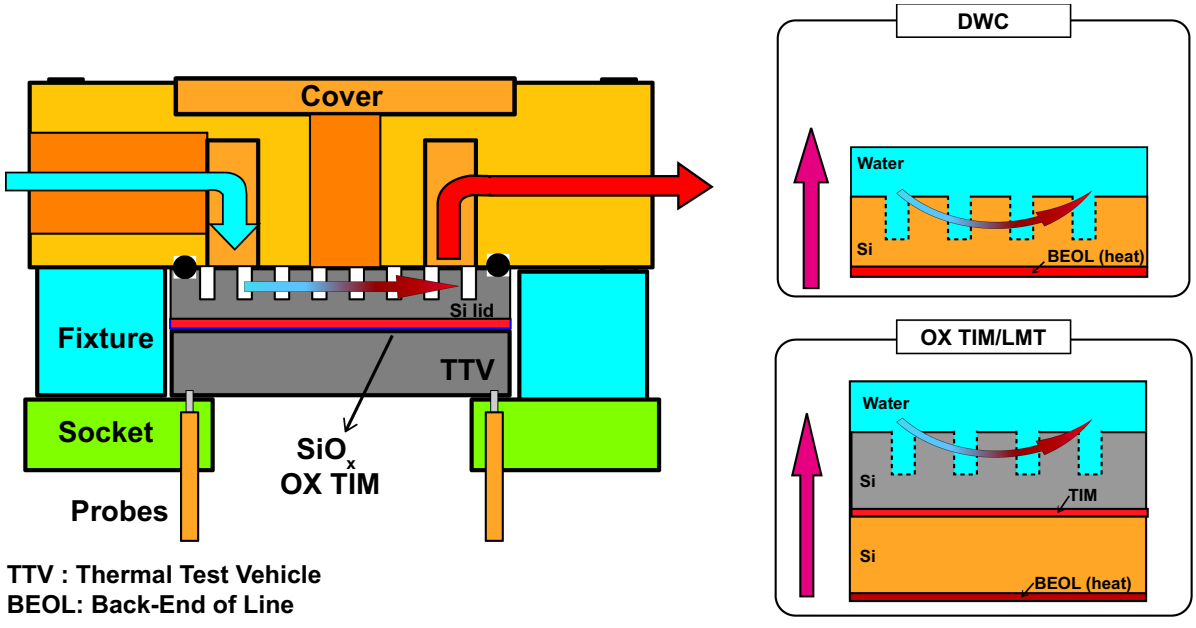

Figure 7. Schematic of the customised pin socket. An o-ring is utilised to achieve water sealing. Two trenches are designed in the cover to create a uniform flat plate flow through the Si pillar array. Right top image shows direct water cooling (DWC) and bottom image shows the addition of SiO_x thermal interface model (OX TIM)/Liquid metal TIM (LTM) (reproduced with permission from [83]).

Table 2. Recent Development in Cooling Techniques for Thermal Management in 3D ICs.

Paper	Approach	Outcome	Year
[85]	Liquid jet impingement/multi-jet backside cooling	Achieves heat transfer coefficients up to 6.25×10^4 Wm^{-2} K^{-1} with a pump power as low as 0.3 W	2018
[86]	Embedded microfluidic cooling (die-per-layer microchannels, inter-tier or through-chip channels)	supports heat fluxes above 10^4 W/cm^2 with <60 K rise; enables active two-phase flow cooling directly within the stack	2024
[87]	Thermal scaffolding with conductive dielectric materials	Reduces footprint penalty from 10% to 5.5% due to 3D thermal scaffolding and simultaneously meets worst-case IR drop constraint of <20 mV at 0.7 V supply and peak temperature constraint of <125 °C	2024
[88]	Temperature-Effect Inversion based thermal management (TEI-LP)	Achieves 17.8% and 16.3% reductions in energy consumption at 50 MHz and 100 MHz respectively	2024
[89]	Nano-engineered thin-film thermoelectric cooling	Thin-film thermoelectric modules offer 100–300% better coefficient-of-performance than bulk devices depending on operational scenarios	2025

5 Electrical performance and interconnect considerations

As semiconductor technology advances towards complex 3D architectures and heterogeneous integration, managing electrical performance and interconnects becomes a critical challenge. The move to stack multiple dies introduces a new set of issues that can have an impact on the reliability and speed of the entire system. This section explores several key considerations in this domain: (i) The degradation of signal integrity and introduction of delays in vertical interconnects like TSVs; (ii) The difficulties in delivering stable power across these stacked layers; (iii) The parasitic effects of TSVs and interposer routing; (iv) Increased crosstalk and noise coupling between tightly packed components; and (v) The crucial need to co-optimise electrical and thermal performance for overall system stability.

3D integration is already delivering link- and system-level gains relevant to automated interconnect planning. A self-timed 3 nm die-to-die (D2D) PHY demonstrates 8 Gb/s per pin at 0.7 V with 77 fJ/bit energy and about 44 Tb/s/mm^2 bandwidth density, indicating single-cycle hop latency at fine pitches [90]. A complementary 9 μm-pitch PAM-4 D2D test vehicle in 5/6 nm reports 16 Gb/s per pin, 10.24 Tb/s aggregate bandwidth, 0.296 pJ/bit, and 17.9 Tb/s/mm^2, showing a tileable, cluster-based path to throughput scaling [91]. Foundry guidance is consistent: the 3D interconnect roadmap targets about a 2× node-to-node gain in energy-efficient performance (EEP) by shrinking SoIC bonding pitch roughly 70% per node, and reports multiple-fold density increases with as much as 87% dynamic-power reduction versus microbump for near-memory stacks, which provides useful bounds for lane count, pitch, and thermal-cooling co-design in automation [92].

At the system level, many-core bandwidth-latency-thermal co-optimisation links practical pitch choices with achievable performance, showing that sub-2 μm vertical interconnects are a feasible threshold for unlocking higher core-to-memory bandwidth under thermal limits [93]. A comparative PPA study across heterogeneous 3D options quantifies technology-choice deltas: hybrid bonding yields up to 81.4% timing improvement versus 2D and 25.8% EDP reduction on commercial CPU-class designs, while signal-integrity analysis map how MIV (sub-micron), face-to-face, and microbump pitches create trade off between crosstalk and signal-to-noise ratio (SNR) for constraint generation [94]. For memory-bound automation, HBM on interposers provides a 4096-bit interface at around 1 GHz achieving roughly 512 GB/s peak bandwidth (Fury X example), illustrating wide-and-slow links that reduce energy per bit within surface capacity constraints [95]. In heterogeneous multi-tier compute-in-memory (CIM), electrical-thermal co-design sweeps identify a TSV diameter sweet spot of 1-3 μm that balances throughput and density with IR-drop and temperature, which is actionable for tier-to-tier channel sizing and thermal-aware routing [96].

In 3D ICs, signal quality through vertical interconnections like TSVs presents significant reliability and performance challenges. These vertical channels are subject to parasitic parameters-resistance, capacitance, and inductance-that degrade signal waveforms and introduce noise [97]. Moreover, the compact stacking of dies intensifies signal latency, which can lead to synchronisation mismatches and impair system timing [98].

Parasitic phenomena intrinsic to TSV structures, especially resistance and capacitance, play a central role in signal loss and propagation delay [99]. As the number of stacked layers grows, the interconnect density rises, leading to shorter inter-layer paths that still exhibit greater signal distortion due to increased

coupling. This can result in timing violations and data integrity issues, especially in high-throughput designs [100].

To alleviate these concerns, multiple engineering approaches are employed. Fine-tuning the physical attributes of TSVs-such as minimising via diameter, selecting low-resistivity materials, and adopting more efficient via geometries help in mitigating signal degradation [100]. Complementary circuit-level techniques, including the deployment of buffers, amplifiers, and clock distribution frameworks, further enhance signal robustness and reduce timing skew [97]. A comparative summary of innovative vertical interconnect solutions-including carbon nanotube (CNT) TSVs, photonic interconnects, and adaptive buffer insertion-is presented in Table 3.

Delivering stable and reliable power across vertically stacked dies remains a key bottleneck in 3D IC architectures. Due to the constrained footprint and elevated current demands, ensuring even voltage distribution becomes increasingly complex as the layer count rises [106]. A major concern in this context is the IR drop-voltage reduction along resistive paths-which can lead to insufficient power delivery in upper tiers and potentially jeopardise system operation [107].

As stacking becomes more aggressive, the interplay of TSV-related parasitic inductance and capacitance increasingly impacts the PDN, creating voltage ripple and transient instability [106]. If left unaddressed, such issues may escalate into performance losses or functional failures under dynamic workloads [107].

To enhance power integrity in 3D ICs, various strategies have emerged. Layer-specific power planes can help in maintaining localised voltage levels and improving power uniformity [106]. Employing low-resistivity materials in power and ground networks and optimising the TSV layout are also effective in minimising resistive losses [107]. Additionally, advanced PDN modelling and simulation techniques can be used proactively to forecast hotspots and guide the design of more resilient power delivery frameworks [99]. Table 4 outlines key innovations in this space, including fine-grained voltage regulation, hybrid integration schemes, and thermal-aware co-design methodologies.

Parasitic effects inherent to TSVs, notably resistance (R), capacitance (C), and inductance (L), pose major design challenges in 3D integrated circuits [113]. These parasitics not only cause signal degradation and delay but

Table 3. Overview of Vertical Interconnect Technologies for Signal Integrity and Delay Improvement.

Paper	Name	Category	Year	Advantages
[101]	TSV Interposer Integrated X-band Filter	Electrical Optimisation Methods	2019	Low insertion loss (2.2 dB), wide bandwidth (2.33 GHz), small group delay variation (52 ps); uses high-resistivity silicon to reduce substrate loss and enhance Q factor.
[102]	CNT-based Tapered TSV Structures	Material Innovation	2022	Tapered single-/multi-wall CNTs reduce crosstalk-induced delay (by ~22.8%) and peak noise; lower power loss and improved transmission/reflection loss vs. Cu-based TSVs.
[103]	Edge Coupler Integrated TSV Optical Module	System-Level Integration	2023	Enhanced signal bandwidth and reduced delay through direct EIC–PIC interconnect using TSVs; low insertion loss (<0.35 dB @ 67 GHz), clean eye diagrams at 112 Gbps.
[104]	Hollow Tungsten TSV (W–TSV)	Structural Optimisation	2024	Reduces thermal-induced stress by 60.3%, keeps surface stress below 31.02 MPa; no KOZ required, enabling denser integration and better signal reliability.
[105]	GNR Interconnect with Buffer Insertion	Routing and Layout Strategies	2025	Simultaneous reduction in interconnect resistance (>30%) and delay (>40%) via optimal buffer placement; improves both signal and power integrity.

Table 4. Summary of power delivery optimisation techniques.

Paper	Name	Category	Year	Advantages
[108]	Hybrid-Bonding 3D IC with Inter-Tier Metal Sharing and MIM Decap Sharing	Material Innovation	2022	Reduces dynamic IR-drop by up to 77 mV; achieves 17 mV less static IR-drop than micro-bumps; up to 76% performance boost.
[109]	Fully Integrated Voltage Regulator (FIVR)-based Power Delivery Methodology for 3D ICs	Electrical Optimisation Methods	2022	5× reduction in power loss and 24× IR-drop reduction in 5-layer 3D stack.
[110]	Hybrid Bonded Backside PDN with nTSVs and CuPads	Structural Optimisation	2023	69% average IR-drop reduction vs. frontside; nTSVs improve IR-drop over μTSVs by 81% (avg) and 77% (peak).
[111]	Iterative Layout-Aware Electrothermal Co-Optimisation (LoM Stack)	Routing and Layout Strategies	2025	6 °C lower temperature in LoM vs. MoL; 54% IR-drop reduction using tighter PDN pitch.
[112]	3D Heterogeneously Integrated Digital DC/DC Power Module for Vertical Power Delivery	System-Level Integration	2025	Power density of 1468 W/in^3, >96% efficiency, <1% voltage ripple, and improved IR loss.

also complicate timing closure and increase the likelihood of timing violations, especially as interconnect density increases with more stacked layers. High resistance and capacitance along TSVs lead to increased RC delay and signal attenuation. Their large size and proximity further cause coupling capacitance between adjacent TSVs, intensifying crosstalk and noise interference. Imperfect TSV processing may introduce defects-for example, resistive opens or bridges-leading to further deterioration of signal quality due to increases in RC delay. In addition, interposer routing introduces additional parasitic load and longer signal paths, which can degrade both signal and power integrity, especially important as system complexity grows [114].

Mitigation strategies include optimising TSV physical parameters (smaller diameter, strategic placement, and selection of low-loss liner materials), use of shielding or guard TSVs, and evolving toward coaxial or advanced CNT-filled TSVs to reduce parasitics and improve high-frequency performance [115,116]. Thorough post-bond testing and redundancy in TSV design also help maintain reliability in large-scale 3D-IC implementations [117,118].

Crosstalk-the undesirable coupling of signals between adjacent TSVs-remains a significant challenge in high-density 3D stacking [119]. Closely packed TSVs, especially those transmitting high-frequency signals, generate electrostatic and electromagnetic interference due to the strong coupling capacitance between them. This can result in signal integrity issues such as increased jitter, false toggling, or data corruption, ultimately limiting achievable bandwidth and performance.

Several factors influence TSV crosstalk, including TSV pitch, diameter, dielectric environment, and routing topology. Embedding ground TSVs between signal TSVs and optimising their spatial arrangement can notably reduce noise coupling. In addition, advanced TSV structures such as CNT-filled, tapered, or coaxial TSVs have demonstrated reductions in crosstalk-induced delay and power dissipation [115,120]. On the algorithmic side, crosstalk-aware channel encoding and adaptive crosstalk avoidance coding further mitigate the risk for highly parallel channels [114]. Table 5 outlines some approaches to mitigate crosstalk and noise issues. These combined materials, physical configurations, and signal processing approaches help preserve signal integrity in future large-scale 3D ICs.

The electrical and thermal behaviours of 3D ICs are deeply intertwined, necessitating a holistic co-design approach. High power densities in stacked dies intensify self-heating and thermal gradients, which affect TSV reliability, induce thermomechanical stress, and may ultimately degrade electrical performance due to increased resistance, leakage, and electromigration. Simultaneously, TSVs can be leveraged as both electrical conductors and thermal conduits; their placement and density thus influence both IR-drop and heat distribution [113].

Co-optimisation techniques-such as thermal-aware floor planning, placement-driven TSV and power grid design, and coupled electro-thermal simulation-are critical for next-generation 3D systems [124]. Recent works have demonstrated that evolutionary floor planning algorithms and iterative layout-aware co-optimisation significantly improve both temperature profiles and IR-drop targets in complex stacks as discussed in the previous section. Incorporating high-thermal-conductivity materials in dielectric and adhesive layers, as well as optimising microchannel cooling proximity to hotspots, produces further benefits at the system level. Ultimately, such integrated co-design methodologies are essential to achieve robust, power-efficient, and high-performance 3D ICs that can strengthen future intelligent computing platforms.

Table 5. Summary of crosstalk and noise mitigation techniques.

Paper	Name	Year	Advantages
[121]	Grounded Shields/Guard Rings	2014	Reduces capacitive coupling by isolating sensitive nets from aggressors and creating a more effective discharging path.
[119]	Optimised Routing (Net Spacing)	2018	Increases the physical distance between TSVs and other signal paths, which diminishes electromagnetic coupling and its resulting crosstalk.
[121]	Differential Signalling	2014	Transmits a signal using a pair of conductors. This method provides superior noise immunity by effectively rejecting common-mode noise that is coupled to both lines.
[122]	Crosstalk Avoidance Codes (CACs)	2017	Involves remapping data bits before transmission in a way that minimises the crosstalk generated. This can reduce crosstalk on TSVs and metal wires by approximately 30% and 50%, respectively.
[123]	Tapered TSV Structures	2023	Utilising TSVs with a tapered shape can effectively lower crosstalk-induced delay, thermomechanical stress, and the power-delay product (PDP).
[119]	Adding Reference (Ground) Vias	2018	Incorporating additional ground vias helps to establish well-defined return paths for the current, which has a significant impact on mitigating crosstalk.

As high-performance computing (HPC) and AI systems continue to scale, the interconnects between processors, accelerators, and memory have become a primary performance bottleneck. High-speed Serializer/Deserializer (SerDes) interfaces, which form the backbone of data centre communication, are now pushing data rates to 56 Gbps, 112 Gbps, and beyond [125,126]. In traditional systems, these electrical signals must travel long distances across printed circuit boards (PCBs) to reach front-panel pluggable optical modules, leading to significant signal degradation, high power consumption, and latency, which collectively limit system bandwidth and scalability [127].

Advanced 3D IC packaging provides a transformative solution to this challenge through the heterogeneous integration of co-packaged optics (CPO). CPO involves placing optical I/O engines on the same package substrate as the primary silicon die, like a switch ASIC or an accelerator. This architecture dramatically shortens the length of the high-speed electrical traces from tens of centimeters to just a few millimetres [127]. The result is a substantial reduction in the power required to drive the SerDes links, improved signal integrity due to lower channel loss, and a massive increase in bandwidth density at the chip edge. By converting high-speed electrical signals to optical signals closer to the source, 3D packaging with CPO effectively bypasses the conventional interconnect bottlenecks that hinder the performance of large-scale computing systems.

The implementation of CPO relies heavily on the capabilities of advanced packaging technologies, including 2.5D and 3D integration, which enable the dense and reliable interconnection of both copper and optical components [128]. For instance, the use of glass core substrates (GCS) is emerging as a key enabler, offering superior dimensional stability and electrical properties needed to support the large package sizes and fine-pitch interconnects required for AI and HPC applications utilising CPO [129]. These advanced packaging techniques are crucial not only for the ASIC-to-optics interface but also for optimising the high-density copper traces and TSVs that are integral to the package design [130]. This synergy between 3D packaging and co-packaged optics represents a critical path for breaking through the memory wall and interconnect-scaling limitations in the next generation of high-performance computers [131].

6 Summary and outlook

3D integrated circuit (3D ICs) technology has evolved significantly since its first commercial deployment in image sensor modules in the late 2000s (Figure 8). The concept was initially driven by the formation of through-silicon vias (TSVs) to enable vertically stacked systems. Since then, 3D ICs have gained momentum in both research and product development. Early industrial adoption focused on applications such as image sensors and DRAM stacking, with high-bandwidth memory (HBM) emerging as a landmark achievement in stacking technology. It has now been nearly a decade since Micron and Samsung began mass-producing HBM for data-intensive AI workloads. Emerging paradigms such as BEOL-compatible oxide-semiconductors, processing-in-memory (PIM) or computing-in-memory (CIM), and neuromorphic computing have further accelerated interest in 3D IC-based computing platforms.

Packaging remains one of the most critical aspects of stacked device technology, requiring highly advanced bonding processes. Although substantial progress has been made in both temporary and permanent bonding techniques, several key challenges still remain. The fabrication of high aspect-ratio (AR) TSVs is particularly demanding as the number of stacked dies increases. Uniform deposition in such TSVs is difficult to achieve due to defect formation during processing, and reliable defect characterisation remains a major hurdle. Companies such as Carl Zeiss and Bruker are developing dedicated metrology tools to address TSV defect detection, while machine learning approaches-including neural network-based frameworks-are being explored to enhance defect analysis.

Other pressing research areas include the handling of carrier wafers, optimisation of temporary/permanent bonding materials, integration of thermal interface materials (TIMs), TSVs alignment, and the co-design of these factors with thermal management strategies. Design consideration of the thermal budget for the bottom die in a stack is mostly lacking in the literature. Incorporating thermal management strategies early in the 3D ICs design flow is essential. Most reported heat transfer models adopt simplified architectures that overlook real-world physical complexities. Developing more sophisticated and realistic thermal transport models is critical for accurately predicting heat dissipation across all layers, with

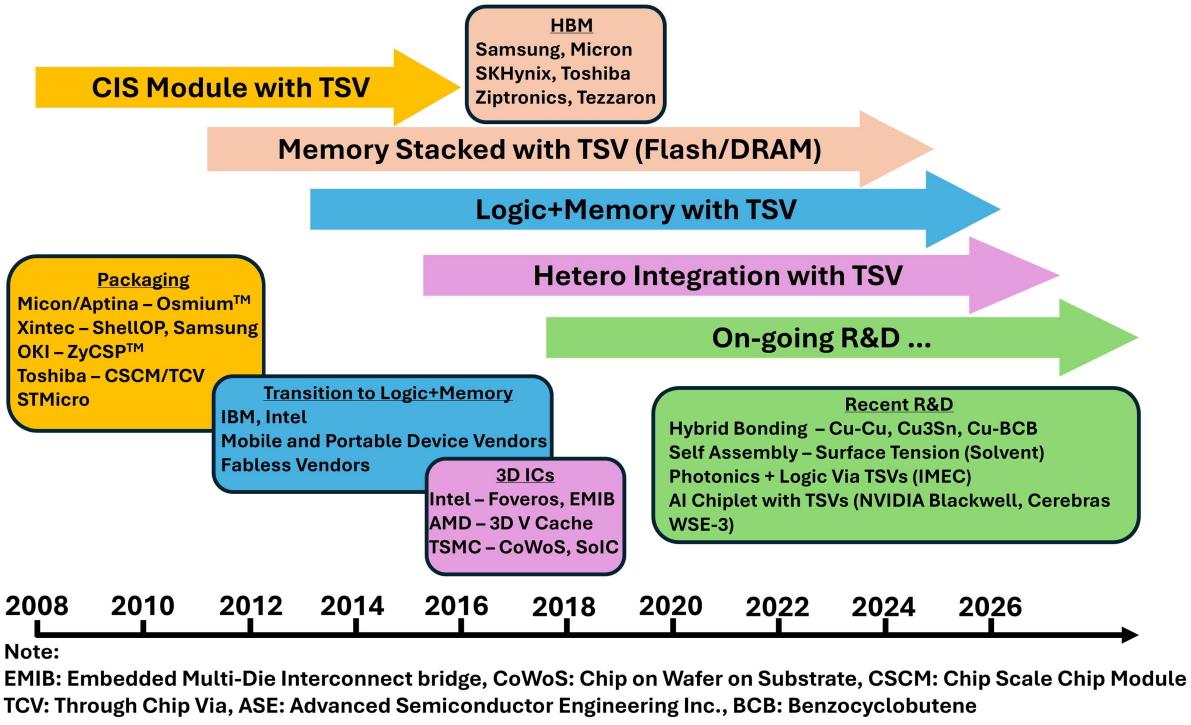

Figure 8. Major timeline of 3D system technology development and future outlook.

particular emphasis on the thermal behaviour of intermediate layers, which is vital for ensuring product reliability.

Although some studies have addressed intermediate-layer thermal management through optimised power delivery network (PDN) architectures, the effective mitigation of localised hotspots in these regions remains largely unexplored. Cooling technologies tailored for 3D ICs are still in their early stages. While microfluidic cooling shows strong potential for stacked systems, it must be co-optimised with other reliability parameters, such as dielectric loss minimisation, to ensure overall system performance. Currently, the major research thrust of 3D ICs technology is focused on optimising electrical and thermal performance and leveraging its advantages through heterogeneous integration (HI). However, for a smooth transition from academia to industry, yield and cost at manufacturing scale must be considered. Multiple models now guide cost-aware flow selection for stacked systems. Taouil's PhD thesis develops yield/cost formulations that capture stack-level defect compounding and the role of pre-/mid-/post-bond test and repair in overall economics [132]. At the system level, Dong and Xie et al. analyse how partitioning choices and integration flows drive total cost, while Chen et al. emphasise the testing component and design-for-test overheads as key levers in cost-effective 3D integration [133,134]. More recently, Jeloka et al. frame these trade-offs in a contemporary system-technology co-optimisation context, highlighting how advances in bonding pitch and power-delivery constraints shift cost/performance break-even points among flows [135]. In parallel, standardisation is progressing: IEEE Std 1838 defines a test-access architecture for three-dimensional stacked ICs, linking cost/yield insights to actionable design for testability (DfT) practice and enabling interoperable test strategies across dies and stacks [136]. Broader adoption of such standards in the design, fabrication, and testing workflows will be an important step toward the large-scale commercialisation of 3D ICs technology.

In conclusion, while 3D ICs present significant fabrication, thermal, and reliability challenges, rapid advancements in simulation, manufacturing, and characterisation techniques are steadily making them a more practical solution for next-generation computing demands. The formation of global 3D ICs research consortia reflects a coordinated push across academia and industry to address these challenges. The development of 3D ICs technology spans multiple engineering disciplines, requiring interdisciplinary collaboration to bring the technology to mainstream consumer applications. This review provides

researchers and practitioners with a consolidated view of the current state of 3D ICs, along with key challenges and future directions for this transformative technology.

Disclosure statement

The authors declare no competing financial interest.

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